3. **a)** We compute $(1 \cdot 1) + (\overline{0 \cdot 1} + 0) = 1 + (\overline{0} + 0) = 1 + (1 + 0) = 1 + 1 = 1$.

b) Following the instructions, we have $(\mathbf{T} \wedge \mathbf{T}) \vee (\neg(\mathbf{F} \wedge \mathbf{T}) \vee \mathbf{F}) \equiv \mathbf{T}$.

5. In each case, we compute the various components of the final expression and put them together as indicated.

For part **(a)** we have

x	y	z	$\overline{x}$	$\overline{x}y$
1	1	1	0	0
1	1	0	0	0
1	0	1	0	0
1	0	0	0	0
0	1	1	1	1
0	1	0	1	1
0	0	1	1	0
0	0	0	1	0

For part **(b)** we have

x	y	z	yz	$x + yz$
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	0	1
0	1	1	1	1
0	1	0	0	0
0	0	1	0	0
0	0	0	0	0

For part **(c)** we have

x	y	z	$\overline{y}$	$x\overline{y}$	xyz	$\overline{xyz}$	$x\overline{y} + \overline{xyz}$
1	1	1	0	0	1	0	0
1	1	0	0	0	0	1	1
1	0	1	1	1	0	1	1
1	0	0	1	1	0	1	1
0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	1
0	0	0	1	0	0	1	1

For part **(d)** we have

x	y	z	$\overline{y}$	$\overline{z}$	yz	$\overline{y}\,\overline{z}$	$yz + \overline{y}\,\overline{z}$	$x(yz + \overline{y}\,\overline{z})$
1	1	1	0	0	1	0	1	1
1	1	0	0	1	0	0	0	0
1	0	1	1	0	0	0	0	0
1	0	0	1	1	0	1	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0	0
0	0	0	1	1	0	1	1	0

9. By looking at the definitions, we see that this equation is satisfied if and only if $x = y$, i.e., $x = y = 0$ or $x = y = 1$.

15. The idempotent laws state that $x \cdot x = x$ and $x + x = x$. There are only four things to check: $0 \cdot 0 = 0$, $0 + 0 = 0$, $1 \cdot 1 = 1$, and $1 + 1 = 1$, all of which are part of the definitions. The relevant tables, exhibiting these calculations, have only two rows.

21. We construct the relevant tables (as in Exercise 13) and compute the quantities shown. Since the fourth and seventh columns are equal, we conclude that $\overline{(xy)} = \overline{x} + \overline{y}$; since the ninth and tenth columns are equal, we conclude that $\overline{(x+y)} = \overline{x}\,\overline{y}$.

x	y	xy	$\overline{(xy)}$	$\overline{x}$	$\overline{y}$	$\overline{x}+\overline{y}$	$x+y$	$\overline{(x+y)}$	$\overline{x}\,\overline{y}$
1	1	1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	1	0	0
0	1	0	1	1	0	1	1	0	0
0	0	0	1	1	1	1	0	1	1

24. **a)** Since $0 \oplus 0 = 0$ and $1 \oplus 0 = 1$, this expression simplifies to x.

b) Since $0 \oplus 1 = 1$ and $1 \oplus 1 = 0$, this expression simplifies to $\overline{x}$.

c) Looking at the definition, we see that $x \oplus x = 0$ for all x.

d) This is similar to part **(c)**; this time the expression always equals 1.

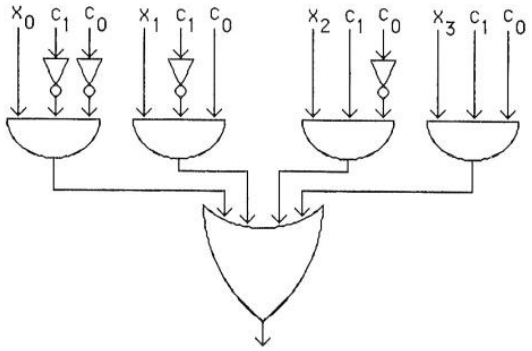
2. **a)** We can rewrite this as $F(x,y) = \overline{x} \cdot 1 + \overline{y} \cdot 1 = \overline{x}(y + \overline{y}) + y(x + \overline{x})$. Expanding and using the commutative and idempotent laws, this simplifies to $\overline{x}\,y + \overline{x}\,\overline{y} + x\,y$.

b) This is already in sum-of-products form.

c) We need to write the sum of all products; the answer is $x\,y + x\,\overline{y} + \overline{x}\,y + \overline{x}\,\overline{y}$.

d) As in part **(a)**, we have $F(x,y) = 1 \cdot \overline{y} = (x + \overline{x})y = x\,y + \overline{x}\,y$.

19. We can set this up so that the value of x_i "gets through" to a final *OR* gate if and only if $(c_1 c_0)_2 = i$. For example, we want x_2 to get through if and only if $c_1 = 1$ and $c_0 = 0$, since the Base 2 numeral for 2 is 10. We can do this by combining the x_i input with either c_0 or its inversion and either c_1 or its inversion, using an *AND* gate with three inputs. Thus the output of each of these gates is either 0 (if $(c_1 c_0)_2 \neq i$) or is the value of x_i (if $(c_1 c_0)_2 = i$). So if we combine the result of these four outputs, using an *OR* gate, we will get the desired result (since at most one of the four outputs can possibly be nonzero). Here is the circuit.



4. This is similar to the previous three exercises. The output is $\overline{(\overline{x}\,y\,z)}(\overline{x}+y+\overline{z})$.

6. We build these circuits up exactly as the expressions are built up. In part **(b)**, for example, we use an *AND* gate to join the outputs of the inverter (which was applied to the output of the *OR* gate applied to x and y) and x.